A 310 nW 14.2-bit Iterative-Incremental ADC for Wearable Sensing Systems

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***Abstract*—This paper presents an energy-efficient ultra-low power incremental analog-to-digital converter (I-ADC) for wearable sensing systems. In order to improve the energy efficiency without sacrificing the conversion resolution and linearity, limited by the use of Nyquist quantizers as in traditional two-step I-ADCs, we propose an iterative I-ADC (II-ADC) that breaks this performance tradeoff by taking advantage of the two-step topology while iteratively reusing the same hardware for both the coarse/fine conversions. As a result, higher SQNR can be accomplished with the same number of conversion cycles, leading to improved energy efficiency. Chopping and dynamic element matching are utilized for low offset and high linearity. Fabricated in 0.18-µm standard CMOS, the proposed II-ADC occupies an active area of only 0.08 mm^2. The chip prototype operating at 4 kHz achieves a SNDR of 87.2 dB over a 25 Hz bandwidth while consuming only 310 nW from a 1-V supply, corresponding to a Shreier and Walden Figure-of-Merit (FoM) of 330 fJ/conv.-step and 166.3 dB, respectively.**

***Keywords*—chopping; dynamic element matching; energy efficiency; incremental ADC; sensor interface; two-step; ultra-low-power; wearable sensing system**

I. INTRODUCTION

The advances in miniaturized devices and ubiquitous computing fostered a dramatic growth of interest in wearable sensors and systems for various clinical usages, and are currently on the verge of explosion for wellness and prevention-oriented healthcare applications. Wearable gadgets, such as chest-band and wrist-band, are widely available in the market for monitoring human activities and other vital signs. The Samsung Simband wearable healthcare and wellness tracker is one of the many examples that promises real time measurements including the wearer's heart rate, blood pressure and body temperature. Another example is the BioStamp Research Connect System which is flexible, bendable and stretchable while capable of collecting raw kinematic and surface bio-potential data, as launched by MC10 Inc. in CES 2016. Yet, the limited battery capacity ultimately sets a major bottleneck that directly jeopardizes the system volume and usage time, which are of utmost importance in such wearable devices [1]. This calls for the development of novel system architectures as well as highly energy efficient building blocks so as to achieve high system performance within a limited power budget.

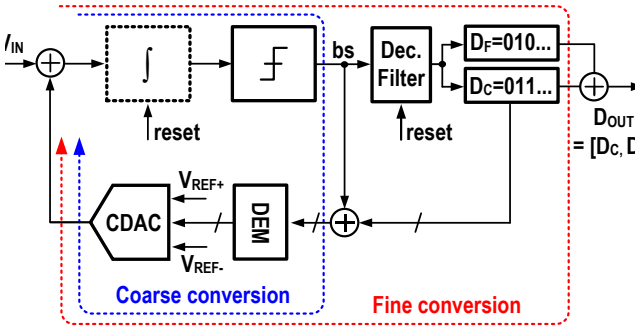

Fig. 1. The system architecture of the proposed II-ADC featuring two-step coarse/fine conversions using the same ADC core without requiring any Nyquist quantizer.

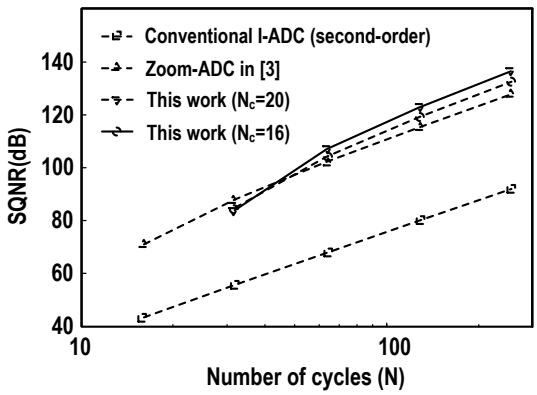

Fig. 2. The SQNR versus number of cycles (N), with the coefficients of the integrators set to one for fair comparison. The proposed II-ADC exhibits an improved SQNR at high resolution when compared with that in [3], which is fundamentally limited by the achievable resolution of the Nyquist quantizer during coarse conversion.

A wearable system mainly consists of three building blocks: 1) front-end sensors; 2) sensor readouts; and 3) data communication. In terms of signal conditioning, even though the MEMS technology has enabled the development of miniaturized sensors that transduce various physical quantities into electric parameters with high energy efficiency, the associated readout circuitry with an analog-to-digital converter (ADC) becomes critical to achieve high system performance. Wearable sensor applications often involve narrow-band signals with frequencies from DC up to few tens of Hz [2-3],

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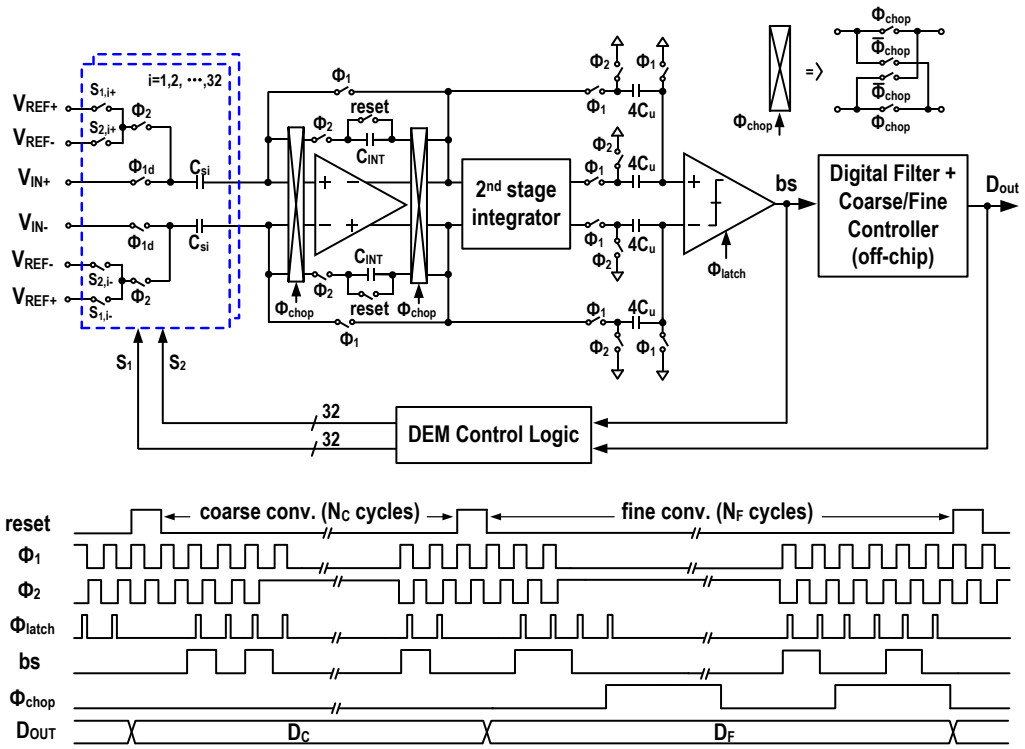

Fig. 3. The simplified schematic of the proposed II-ADC and the associated timing diagram.

and the ADC should attain high accuracy to quantize weak bio-signals even in the presence of high DC offset and flicker noise.

The Incremental ADC (I-ADC) is normally considered as the best candidate in low-frequency high-resolution sensor interfaces, owing to its advantages of high accuracy, high linearity, low offset and low power dissipation. The equivalent number of bits (ENOB) of an incremental modulator depends on the order of the loop filter, the number of clock cycles per sample, the resolution of the quantizer and the digital post processing. In high resolution applications, higher order modulators show better energy efficiency even in the presence of multiple integrators since the required number of clock periods to achieve the same resolution can be much reduced, but at the expense of increased design complexity for maintaining the system stability.

Recently, two-step topologies including the extended counting [4] and zoom-ADC [3] demonstrate ~10x energy improvements compared to the traditional implementation through the reduction of the number of conversion cycles with coarse/fine converters. However, both of them require the use of Nyquist conversion (i.e. SAR) which only reaches a limited accuracy (e.g. ENOB < 5b in [3]) as a result of offset, gain and linearity errors without calibration. To mitigate the above problems, this paper proposes an iterative incremental ADC (II-ADC) by taking advantage of the two-step topology to iteratively reuse the same ADC core for both the coarse/fine conversions. Consequently, we eliminate the requirement of a Nyquist quantizer while securing high resolution with improved energy efficiency.

II. Architecture of the Proposed II-ADC

Fig. 1 shows the system architecture of the proposed II-ADC which iteratively performs two-step conversions with identical integrators, comparators and feedback capacitive digital-to-analog converter (CDAC). In order to achieve high linearity and relaxed implementation complexity, we choose a 1-bit quantizer and a second-order loop filter as the converter core. The references V_{REF+} and V_{REF-} are dynamically adjusted using the CDAC for fine conversion. During coarse conversion, it operates for N_C cycles as in conventional second-order I-ADC to generate a bitstream *bs* subsequently processed by the decimation filter. The coarse result (D_C) controls the feedback signal to approach the input via the CDAC, effectively shrinking the quantization region by 2^{D_C} times. The II-ADC then operates for N_F cycles using the same hardware for fine conversion. The combination of D_C and D_F contributes to the final output D_{OUT}. The decimation filter incorporates two cascaded counters reused in both steps.

Fig. 2 shows the theoretical signal-to-quantization-noise (SQNR) versus the number of cycles N of the proposed II-ADC with a conventional second-order I-ADC and the zoom-ADC from [3], where we define N as the number of oversampling clock periods within one conversion cycle. The coefficients of the integrators are set to one for fair comparison. Furthermore, the number of cycles to reach a certain SQNR can directly influence the associated energy efficiency. For example, for the same SQNR N can be significantly reduced in the proposed II-ADC when compared with the conventional I-ADC. On the other hand, when compared with the zoom-ADC in [3], the II-ADC is a bit worse at low resolution due to the increased

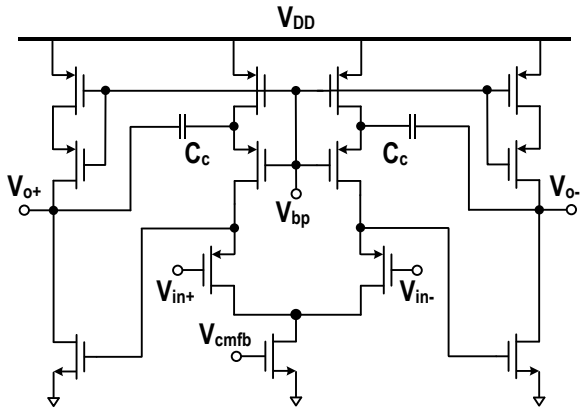

Fig. 4. Schematic of the amplifier in the integrator (CMFB not shown).

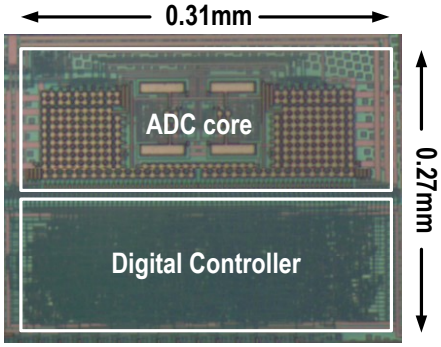

Fig. 5. The die micrograph of the proposed II-ADC occupying an area of 0.08 mm^2.

number of coarse conversion cycles. However, the coarse conversion resolution in [3] is mainly limited by the Nyquist quantizer. Consequently, as the ADC resolution requirement increases, the performance of the II-ADC gradually surpasses that obtained by [3] as a result of the reduced number of fine conversion cycles required to procure the same SQNR.

III. Circuit Implementation

Fig. 3 shows the simplified schematic of the implemented fully differential II-ADC with the corresponding timing diagram. We adopt a second-order feed-forward topology to reduce the output swing and hence avoid saturation of the first integrator. The total input sampling capacitance C_S is 2.8 pF designed to suppress the thermal noise. The unit capacitor C_u is 44fF using MIM capacitors. With N_C=16, we choose 32 unit capacitors to ensure a 5-bit resolution in the coarse conversion, further utilized to adjust the reference for fine conversion. Before each conversion, we reset both integrators. During the sampling phase Φ_1, the input voltage is sampled on all the 32 elements of the CDAC, and the first integrator is in the unity-gain configuration. During the integration phase Φ_2, all the 32 elements are connected to either V_{REF+} or V_{REF-} for coarse conversion, depending on the value of *bs*. While in fine conversion, upon the results of D_C, only k elements are connected to either V_{REF+} or V_{REF-}, transferring an amount of charge proportional to $V_{IN} \pm k\cdot(V_{REF+}-V_{REF-})/32$ to the integration capacitor (2 pF). Dynamic element matching (DEM) controls the switching of the 32 elements in fully differential mode, denoted as $S_{1,2+}$, $S_{1,2-}$ in Fig. 3. To alleviate the accumulation of the offset voltage at the input terminal in the first integrator, that inevitably causes large errors, we adopt a chopping technique to suppress the low-frequency noise (especially the 1/f noise) by swapping the input polarities of the integrator every 8 cycles to effectively overcome the inherent offset.

TABLE I. Power Breakdown of the Proposed II-ADC

Building Block	Simulated	Measured
Ctrl. Logic	61 nW	77 nW
Clock Gen.	19 nW	
CDAC	63 nW	234 nW
First Integrator	90 nW	
Second Integrator	44 nW	
Comparator	22 nW	
Total	299 nW	311 nW

In the proposed II-ADC, the overall linearity is mainly limited by the multi-bit feedback CDAC, which is induced by the mismatches of the CDAC elements. We adopt data weighted averaging (DWA), which is a fast DEM method exhibiting first-order noise shaping, to effectively suppress the mismatch errors. However, the residue mismatch error is highly dependent on the number of averaging cycles. As validated by the behavior model, with a capacitor mismatch of 2%, it requires at least 40 averaging cycles to suppress the mismatch error to below -95 dB (so that the ADC resolution is thermal noise limited), which sets the lower bound for the number of cycles in fine conversion. In this work, N_F is set to 64 to simultaneously suppress the CDAC mismatch and SQNR errors and achieve the required resolution.

In order to reduce the power without sacrificing the signal bandwidth, the amplifier in the integrator employs a two-stage architecture using indirect compensation [5]. Fig. 4 depicts the transistor-level schematic of the amplifier. Different from the traditional miller compensation, we connect the compensation capacitor C_c to an internal low impedance node in the first stage, relieving the second stage from dissipating an unnecessarily high power (normally $g_{m2}>5g_{m1}$) to push the second dominant pole away from the unity-gain bandwidth. Here, the second stage draws comparable current with the first stage (~30nA) while achieving a DC gain, GBW and phase margin of 84.6 dB, 59 kHz and 65°, respectively, at an estimated effective load capacitance of 3 pF. These performances are sufficient for the 15-b II-ADC to operate at an oversampling frequency of 4 kHz. The amplifier only consumes a total of 90 nW including the power of the common-mode feedback (CMFB) circuit.

IV. Measurement Results

Fig. 5 shows the die micrograph of the proposed II-ADC, fabricated in a 0.18-μm standard CMOS process, with an active area of 0.08 mm^2. A FPGA implements the digital filter and coarse/fine controller for flexibility. The 4 kHz clock is provided externally. The output *bs* was post-processed in Matlab. The ADC consumes 310 nW at 1-V supply. V_{REF+} and V_{REF-} are 1 V and 0 V, respectively, resulting in a differential full-scale input range of 2 V. Table I illustrates the simulated

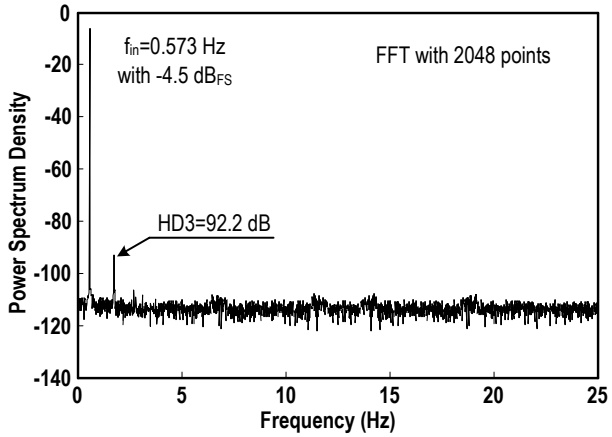

Fig. 6. Measured output spectrum of the proposed II-ADC with an input frequency of 0.573 Hz at -4.5 dB_{FS}, showing an SNDR and HD3 of 87.2dB and -92.2dB, respectively.

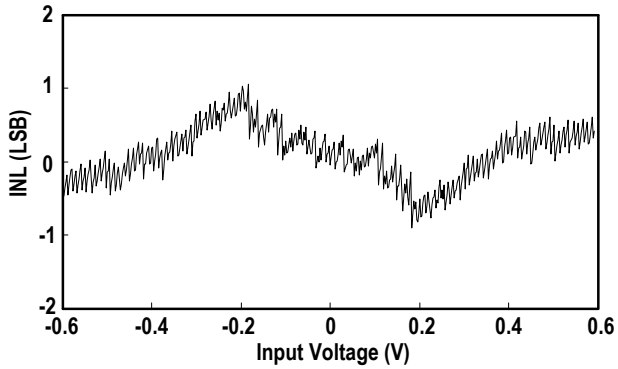

Fig. 7. Measured INL of the proposed II-ADC with ±0.6V input achieving an INL of -0.9/1.1 LSB (with DEM).

power breakdown of each building block. The power of two integrators burns nearly half of the total power. Fig. 6 plots the measured spectrum (FFT with 2048 points) for a -4.5 dB_{FS} sinusoid input at 0.573 Hz. The measured SNDR and third harmonic distortion (HD3) are 87.2dB and -92.2 dB, respectively. Fig. 7 shows that the proposed II-ADC achieves an INL of -0.9/+1.1 LSB with an input range of ±0.6 V.

Table II shows the performance summary and comparison with recent state-of-the-art I-ADCs targeting similar applications, with the Shreier and Walden FoM expressed as,

$$\mathrm{FoM}_S = SNDR + 10log\left(\frac{1}{2^{Power \times Conv.time}}\right) \quad (1)$$

$$\mathrm{FoM}_W = \frac{Power \times Conv.time}{2^{ENOB}}. \quad (2)$$

The resolution of the proposed II-ADC is up to 14.2 bits, with the fine conversion contributing to roughly 9.2 bits with 64 cycles. The total power consumption is only 310 nW. The $\mathrm{FOM_S}$ and $\mathrm{FOM_W}$ are 0.33 pJ/conv.-step and 166.3 dB, which are superior when compared with those in [6] and [7]. When compared with [3] that requires a Nyquist quantizer with limited resolution, this work proposes a two-step II-ADC with a comparable performance within a small area.

TABLE II. PERFORMANCE SUMMARY AND COMPARISON

Parameters	[3] JSSC'13	[6] ISSCC'13	[7] JSSC'15	**This work**
Technology(nm)	160	160	65	**180**
Architecture	SAR+I-ADC	I-ADC	Two-step I-ADC	**II-ADC**
Area(mm^2)	0.375	0.45	0.2	**0.08**
Loop filter order	2	2	2+1	**2**
Supply(V)	1.8	1	1.2	**1**
Power(μW)	6.3	20	10.7	**0.31**
Conv. time(ms)	40	0.75	2	**20**
OSR	2048	500	192	**80**
Input range	1.8	0.7	2.2	**1.2**
C_{IN}(pF)	10.2	0.5	8	**2.8**
ENOB(bits)	19.6	13.3	14.8	**14.2**
SNDR(dB)	119.8	81.9	90.8	**87.2**
INL(LSB)	-6.3/6.3	-0.6/0.4	-0.9/0.8	**-0.9/1.1**
$\mathrm{FoM_S}$(dB)	182.7	157.1	164.5	**166.3**
$\mathrm{FoM_W}$(pJ/conv.-step)	0.32	1.5	0.76	**0.33**

V. CONCLUSIONS

This paper presented an ultra-low power high resolution two-step II-ADC. The chip prototype fabricated in a standard 0.18-μm CMOS technology occupying an active area of 0.08 mm^2. It scores a measured SNDR of 87.2 dB with a signal bandwidth of up to 25 Hz, while dissipating only 310 nW under a 1-V supply. This work accomplishes small area and excellent $\mathrm{FoM_S}$ and $\mathrm{FoM_W}$ when compared with the state of the art, demonstrating an ultra-low-power high-resolution ADC with both high energy- and area-efficiency suitable for wearable sensing applications.

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